ABSTRACT

A low resistance buried back contact for SOI devices. A trench is etched in an insulating layer at minimum lithographic dimension, and sidewalls are deposited in the trench to decrease its width to sublithographic dimension. Conducting material is deposited in the trench, which serves as a low-resistance contact to the back side of the device. In another embodiment, the trench-fill material is separated from the device by an insulating layer, and serves as a back gate structure.